A Fully Integrated Gearbox Capacitive DC/DC-converter in 90nm CMOS: Optimization, Control and Measurements

Tom Van Breussegem
ESAT-MICAS, K.U.Leuven Belgium
Kasteelpark Arenberg 10, B-3001 Heverlee
Email: tvanbreu@esat.kuleuven.be

Michiel Steyaert
ESAT-MICAS, K.U.Leuven Belgium
Kasteelpark Arenberg 10, B-3001 Heverlee
Email: michiel.steyaert@esat.kuleuven.be

***Abstract*—This paper presents a fully integrated capacitive DC/DC-converter with a gearbox type topology. By merging multiple topologies the output voltage range is increased. The dual loop digital control improves load regulation compared with a conventional hysteretic control and reduces ripple under low load operation. The converter was implemented in a 90nm CMOS technology and measurements are presented.**

I. Introduction

Converters using nothing but switches and capacitors have grown in importance, especially in the field of fully integrated converters. This paper discusses the gearbox principle that enables a broad output voltage range and presents two converter topologies for this purpose. Next to this the nested loop control ensures high efficiency over a broad range and a reduction of the output voltage ripple at low loads. In Section II the Topology choice of the converter is justified. In Section III the control method is discussed. Finally in Section IV the measurement results are presented while verifying the design goals.

II. Topology

In [1] the output impedance model is presented: a capacitive converter can be modeled as an ideal voltage source with a non-zero output impedance. At rather low switching frequencies, if the system time constants are smaller than the switching period, the output impedance is inverse proportional with the switching frequency and with the total amount of charge transferring capacitance. The converter is operating in the Slow Switching Limit (SSL). At high switching frequencies the system's time constants exceed the switching period and the parasitic resistances in the circuit dominate the output impedance, this region is called the Fast Switching Limit (FSL). It is clear that a capacitive DC/DC-converter has a fixed ideal Voltage Conversion Ratio (iVCR). The converter can attain this iVCR only with help of a zero output impedance or when no current is delivered to the load. In a more practical case the output impedance is non zero but kept as small as possible to attain a high efficiency. In [2] topologies are characterized by means of K_c and K_s. These topology constants reflect how efficient topologies use resp. their capacitors and switches. The smaller the constants the better. Therefore when comparing capacitive converter topologies, these topology constants are taken into account.

As mentioned in the previous paragraph, a DC/DC-converter is bounded to the characteristic iVCR of the topology of the converter. This means that a lower VCR can be generated but at the cost of efficiency. Because the ratio between the actual VCR and the iVCR is the upper bound for the maximum efficiency [1]. By merging multiple topologies into a single DC/DC-converter, the converter has multiple iVCR so that a broader range of output voltages can be generated at high efficiencies. In order to achieve a certain conversion ratio, one can choose between more than one topology. In Fig. 1 til 4, four topologies are shown. In each figure both phases of these two phase converters are represented. The topologies II and III are quite common used topologies ([3] [4]). Topologies I and IV are proposed as alternatives in this paper.

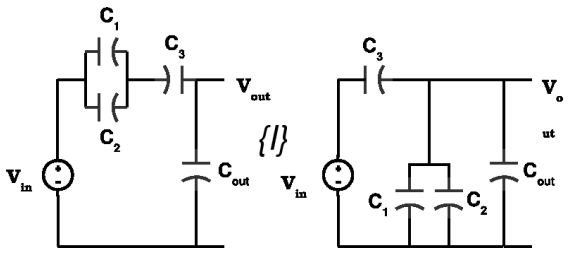

Fig. 1. Schematic representation of Topology I: 2-3 Mak

When implementing two different topologies in a unique converter some considerations are of primary concern. First the efficiency of the topologies, secondly the overhead that is invoked by combining those two topologies. The efficiency of the topologies can be compared based on K_s and K_c. One can see that Topology I and II have equal output impedance for equal switch size and switching frequency constraints and also Topology III and IV perform equaly. Topology I and II have

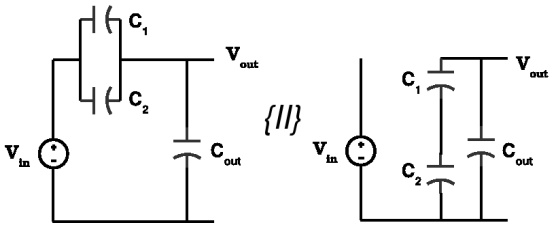

Fig. 2. Schematic representation of Topology II: 2-3 Spd

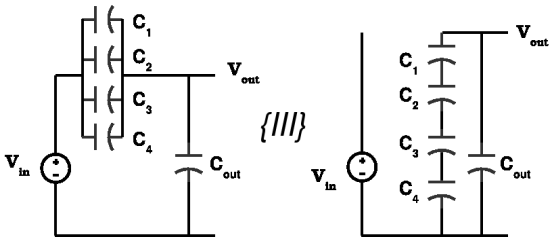

Fig. 3. Schematic representation of Topology III: 4-5 Spd

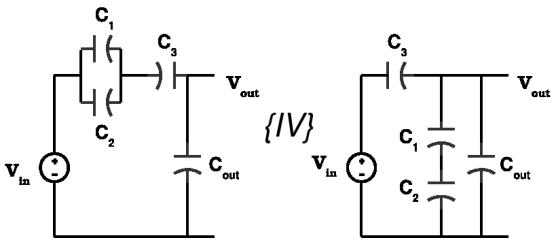

Fig. 4. Schematic representation of Topology IV: 4-5 Mak

$K_c = 0.44$ and $K_s = 5.44$, topology III and IV have $K_c = 0.64$ and $K_s = 6.76$. This means that from a performance point of view any combination of Topology I-IV or I-III or II-IV or II-III are equivalent.

The overhead depicts the number of extra switches that is necessary when adding an extra topology. The overhead is expressed as a percentage of the switches, which are not in common for both topologies, with respect to the total number of switches. The following conclusions are made: Combining Topology I and IV leads to 3 extra switches on a total of 12 switches. Combining Topology II III leads to 5 extra switches on a total of 16 switches. Combining Topology II and IV leads to 10 extra switches on a total of 18 switches. Combining Topology I and III leads to 13 extra switches on a total of 20 switches. It is clear that a gearbox, shown in Fig. 5, built from Topology I and IV has a considerable area benefit compared to a combination of the other topologies. This is not only be reflected in a reduced area but as well in less complex clocking schemes. Especially the presence of a common phase will lead to simplified control implementation.

III. Control

An ideal DC/DC-converter behaves as an ideal voltage source thus maintains a constant output voltage under all possible circumstances. It has been shown in the previous

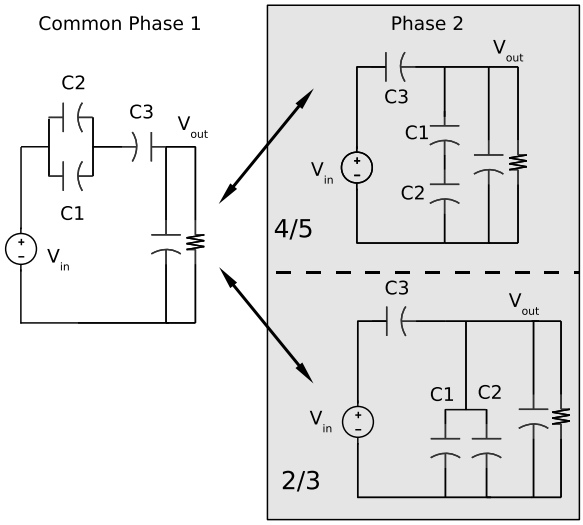

Fig. 5. Implemented converter structures

section that a capacitive DC/DC-converter behaves as an ideal voltage source (which is related to the input voltage by means of the iVCR N) with a non zero output impedance. When a change in load occurs this is anticipated on by means of a change in output impedance to mimic an ideal voltage source. The output impedance is controlled through frequency modulation in SSL [5] [4]. In [6] it has been shown that at high switching frequencies the output ripple of a capacitive DC/DC-converter is additionally reduced because of the RC-filter that is formed by the channel resistance of the switches and the output capacitor. Thus it would be beneficial to switch at high efficiencies even for low loads. This can be done by reducing the flying capacitance under these loads. Therefore a dual control method is implemented shown in Fig. 6. It consists from a frequency modulation loop by means of a hysteretic controller and a loop changing the amount of flying capacitance by a FSM based controller, called the RRL. Both loops are discussed in the next paragraphs.

A. Hysteretic Control

Hysteretic controllers are extremely suitable for use in capacitive DC/DC-converters. During a two phase interval, each capacitor accumulates charge and deliveres it to the load. Activating such a sequence will initiate charge transfer to the load. Charge must only be transferred if there is a lack of charge on the output capacitor thus only when the output voltage is to low.

B. Ripple Reduction Loop

At low loads the ripple can be quite high due to the low switching frequencies and the decreased influence of the parasitic channel resistance of the switches. Therefore it would be beneficial if the switching frequency would be high at low loads as well. Higher switching frequencies imply however that the delivered power is also higher thus we need a technique to increase the switching frequency and keeping the delivered charge constant. This can be done by reducing

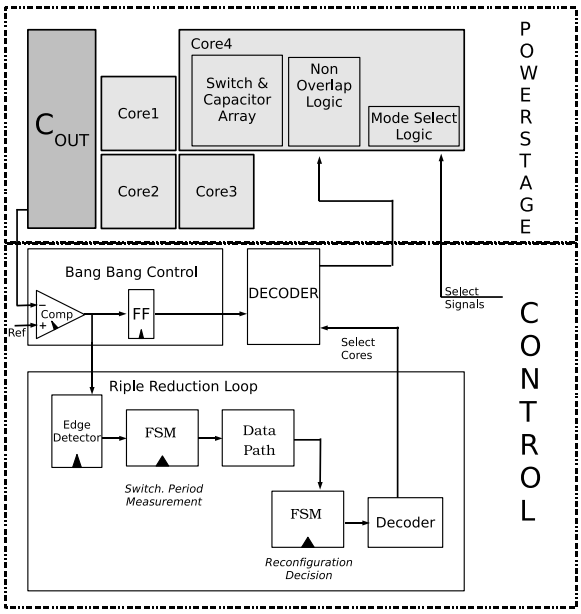

Fig. 6. Schematic system overview

the amount of flying capacitance compared with the amount of output buffer capacitance (Eq. 1). This is achieved by fragmenting the charge pump in four equivalent parallelled charge pumps. In this way parts of the charge pump can be de-activated for compensating the switching frequency increase.

$$Ripple \sim \frac{I_{load}}{2C_{out}f_s} \quad (1)$$

The RRL can be implemented without interfering in the primary hysteretic control loop. The switching frequency is measured by means of two fsm's. These fsm's will detect a low frequency and decide (hard coded) whether a higher frequency is feasible. The fsm's will deactivate part of the charge pump and therefore the hysteretic controller will increase the switching frequency.
If the switching frequency rises and crosses a hard coded boundary the fsm's will detect this and activate the different charge pumps one by one until the switching frequency crosses the frequency boundary again and enters the safe zone.

IV. Measurements

A. Efficiency

It has been explained in previous sections that the converter (shown in Fig. 12) has two different modes corresponding with distinct topologies. Each mode is characterized separately. Efficiency is measured for both nominal input voltages: 1.2V and 1.0V. The output voltages corresponding with the voltage conversion ratios that are implemented in the gearbox are 0.85V/0.72V for the 1.2V input and 0.7/0.6V for the 1.0V input. The measurements were performed with a constant external current load.
In Fig. 7 a) the measurements are shown for the 1V input-case, in Fig. 7 b) for the 1.2V input case. Efficiency remains above 80% for a 300μW up to 4.9mW load. But above 80μW-40μW efficiency is better than ideal linear regulator for resp the 4/5 and the 2/3 mode. When a 1.0V is applied one can see that the DC/DC-converter performs better than an LDO over the power range down to 30μW. A peak efficiency of 87% is achieved 2.7mW from a 1.2V input.

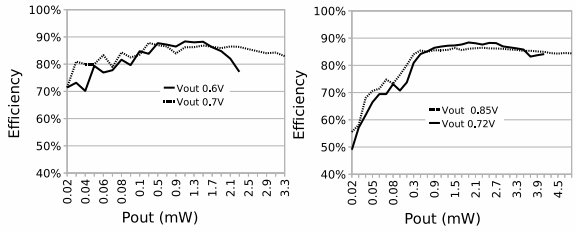

Fig. 7. Efficiency measurements of the gearbox converter a) Vin = 1.0V b) Vin = 1.2V

B. Varying output voltage

Thanks to the gearbox principle high efficiency is maintained over an extended output voltage range this is demonstrated in Fig. 8. The converter is measured for a 1.2V input voltage and a 3mA load. The control voltage is swept so that the output voltage varies between 0.85V and 0.5V. With a single topology the efficiency remains above 80% between 0.85V and 0.75V, thanks to the merged topology-gear box approach this range is extended down to 0.65V. Over the whole range, the merged topology approach remains at least 10% above the maximum efficiency of an ideal linear regulator. In Fig. 9 the Efficiency Enhancement Factor (EEF) [7] is plotted for this case. A maximum EEF of 33% is achieved.

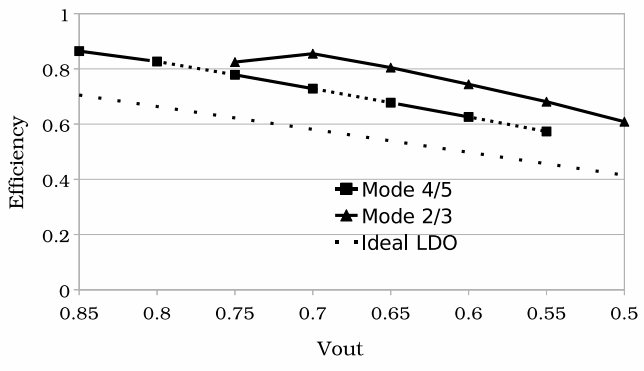

Fig. 8. Efficiency of the converter subject to constant load and varying control voltage

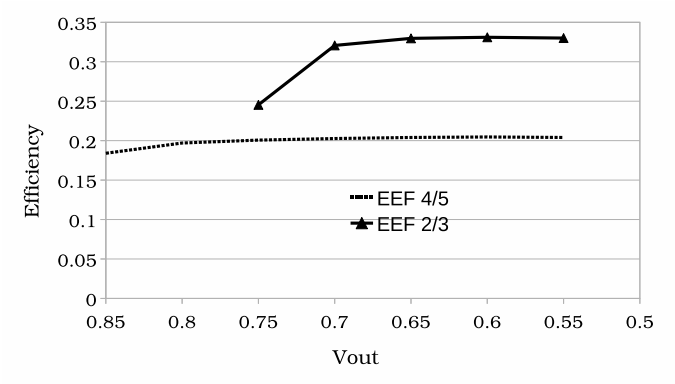

Fig. 9. Efficiency Enhancement Factor of the converter subject to constant load and varying control voltage

C. Varying input voltage

This converter functions properly for voltages down to 0.7V This is demonstrated in Fig. 10 . For an input voltage range between 0.7V and 1.2V, a load current of 1mA and in the 4/5-mode, efficiency remains higher than 80%.

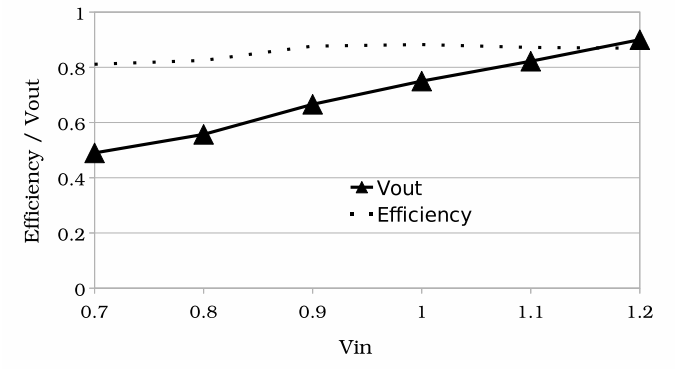

Fig. 10. Efficiency an output voltage in function of varying input voltage

D. Load regulation

For both the 4/5 as the 2/3 mode, a load step was applied at 1MHz. The load step varied the load current between 1.86 mA and 0.186mA. This was done once while the RRL was bypassed and once when the RRL was activated. The measurement of the 4/5 Mode is shown in Fig. 11

In both cases very fast regulation is achieved. In case RLL is bypassed, the response to the load change was quasi instantaneous taking less than 10ns. The influence of the load-step on the RMS output voltage is not neglectable: 20mV. By activating the RRL, the recovery time increases to up to 50ns but the load regulation is much better. The change in RMS voltage was less than 5mV. This demonstrates the benefits of the RRL not only on the reduction of ripple but also on the load regulation specifications. Power measurements prove that the use of the RRL has no influence on the power conversion efficiency of the system.

The efficacity of the RRL can be observed in first place by analyzing the switching frequency under RRL regime and regular regime. If we analyze the 2/3 mode, one can see that the RRL reduces the ripple with a factor 2 by means of increasing the switching frequency and thus deactivating halve of the active charge pump compared with the bypassed regime. Similar behavior can be observed in the 4/5 mode. In both cases power conversion efficiency is not affected.

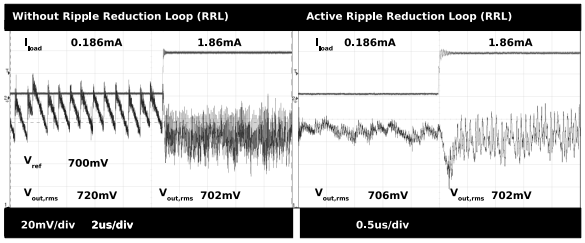

Fig. 11. Effect of a load step on the converter output voltage a) No RRL b) With RRL

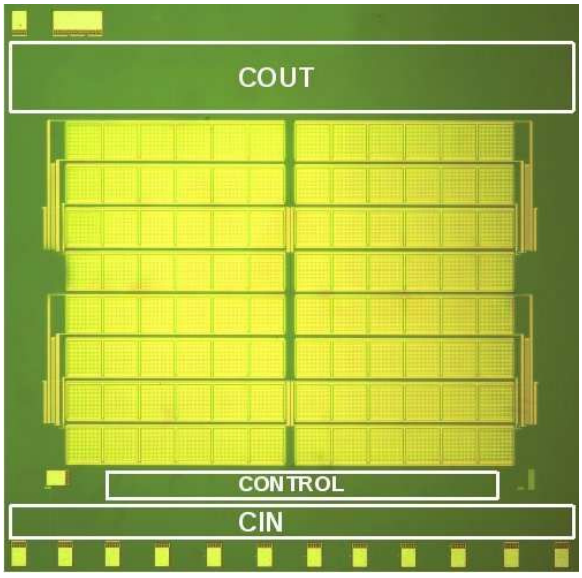

Fig. 12. Micro-photograph of the chip

V. Conclusion

A fully integrated capacitive DC/DC-converter with a gear-box type topology is presented. By merging multiple topologies the output voltage range is increased. The dual loop digital control improves load regulation compared with a conventional hysteretic control and reduces ripple under low load operation.

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REFERENCES

[1] M. Makowski and D. Maksimovic, "Performance limits of switched-capacitor DC-DC converters," in *Proceedings of IEEE Power Electronics Specialists Conference*, 1995, pp. 1215 – 1221.

[2] M. Seeman and S. Sanders, "Analysis and Optimization of Switched-Capacitor DC/DC Converters," *Power Electronics, IEEE Transactions on*, vol. 23, no. 2, pp. 841–851, March 2008.

[3] J. Kwong, Y. Ramadass, N. Verma, and A. Chandrakasan, "A 65 nm Sub-V_t Microcontroller With Integrated SRAM and Switched Capacitor DC-DC Converter," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 1, pp. 115–126, 2009.

[4] M. Seeman, S. Sanders, and J. Rabaey, "An ultra-low-power power management IC for energy-scavenged Wireless Sensor Nodes," *Power Electronics Specialists Conference*, pp. 925–931, 2008.

[5] T. Van Breussegem and M. Steyaert, "A 82% efficiency 0.5% ripple 16-phase fully integrated capacitive voltage doubler," in *2009 Symposium on VLSI Circuits*, June 2009, pp. 198 –199.

[6] G. Perigny, R.; Un-Ku Moon; Temes, "Area efficient CMOS charge pump circuits," 2001, pp. 492–495.

[7] M. Wens, K. Cornelissens, and M. Steyaert, "A fully-integrated 130nm CMOS DC-DC step-down converter, Regulated by a Constant On/Off-Time Control System," in *34rd European Solid State Circuits Conference*, 2008, pp. 62–65.